

Amendments to the Drawings:

Replacement drawings prepared by a competent draftsman are included as an appendix. Applicants request that these drawings replace the figures currently in the application. No changes have been made to the content of the drawings and no new matter has been added. Therefore, no marked up sheets have been included.

REMARKS/ARGUMENTS

After entry of this amendment, claims 1-20 will remain pending in this application. Claims 1, 3-6, 9-12, and 14-18 have been amended. The dependencies of claims 10, 11, and 15-17 have been corrected. Claim 18 has been amended to correct a typographical oversight. Support for the amended claims can be found in the specification. No new matter has been added.

Claims 1-5, 9-13, and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Ellersick et al., United States patent number 6,044,122. (Ellersick.) Claims 8, 14, 15, and 17-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ellersick. Reconsideration of these rejections in light of these amendments and remarks and allowance of all the pending claims is respectfully requested.

Obviousness-Type Double-Patenting Rejection and Statement of Substance of Interviews

The pending office action incorrectly rejects claims 1 and 18 of the pending application on the grounds of non-statutory double-patenting over claims in patent application number 10/779,408. During a phone call with the Examiner it was agreed that the correct application number is 10/799,408.

Application 10/799,408 was filed on the same date as this pending application number 10/799,409, specifically, March 12, 2004. Accordingly, application 10/799,408 is not prior art to this application and cannot be the basis of an obviousness-type double-patenting rejection. Reconsideration of this rejection is respectfully requested.

The dependencies of claims 10, 11, and 15-17 were discussed in a phone conversation between the Examiner and the Undersigned on or about June 20, 2006. It was agreed that the dependencies of these claims were incorrect. The dependencies of claims 10, 11, and 15-17 have been corrected in the claim listings above.

Claim 1

Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Ellersick. But Ellersick does not teach each and every element of this claim. For example, claim 1 as amended, recites "a first series of delay elements including a first delay element coupled to receive a reference clock input;...a second series of delay elements including a second delay element coupled to receive an output of the input buffer, each delay element having an input; and a first register having a clock input coupled to an output of the second series of delay elements." Ellersick does not provide these features.

The pending office action cites Figures 1-10 of Ellersick as teaching each and every element of this claim. (See pending office action, page 6, second paragraph.) But Ellersick does not provide a second series of delay elements and a first register as required by the claim.

Rather, Ellersick in Figure 3 teaches the use of only one series of delay elements, specifically elements 70a-70h. (See Ellersick, Figure 3.) The input of this series of delay elements couples to a reference clock input and its output couples to a phase detector 88. (*id.*) Accordingly, the delay elements 70a-70h of Ellersick Figure 1 roughly correspond to the first series of delay elements recited in this claim. Therefore, these elements cannot be separated to read on both the claimed first and second series of delay elements. Moreover, Ellersick does not provide a first register having a clock input coupled to an output of the second series of delay elements as required. For example, flip-flop 90 in Figure 3 has a clock input coupled to receive the reference clock on line 31. (*id.*) For at least these reasons, claim 1 should be allowed.

Claim 18

Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Ellersick. But Ellersick does not show or suggest each and every element of this claim. For example, claim 18, as amended, recites "delaying the reference clock signal using a first number of delay elements...and delaying the data strobe signal using a second number of delay elements." Ellersick does not provide this feature.

The pending office action recognizes that Ellersick does not show or suggest delaying the data strobe signal using a second number of delay elements as required. (See pending office action, page 10, last paragraph.) The office action states that it would be obvious to add this feature to Ellersick to "ensure reliable data transfer." (See pending office action, page 11, first paragraph.)

But Ellersick does not delay a data strobe signal using a second number of delay elements as required by the claim. Rather, in Figure 8, Ellersick shows a data sampler circuit including eight sampling flip-flops 122a-h. (See Ellersick, Figure 8 and column 10 and lines 31-33.) Ellersick uses a sampling technique that does not require shifting a data strobe signal using a second number of delay elements. Accordingly, it is not obvious to combine shifting a data strobe signal using a second number of delay elements with the teaching of Ellersick.

For at least these reasons, claim 18 should be allowed.

Other claims

Claim 9 should be allowed for similar reasons as claim 1. Specifically, Ellersick does not teach the required first delay line. The other claims depend on one of the above claims and should be allowed for similar reasons and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

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PATENT

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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